Honeywell

AMPA/B-M

MATRIX PRINTER SUBSYSTEM MAINTENANCE

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MATRIX PRINTER SUBSYSTEM MAINTENANCE

1. INTRODUCTION

This publication provides information for the AMPA (300-baud) and the AMPB (1200-baud) Matrix Printers. The printers operate on the Honeywell 4500 computer system through the Model AXSP11 Teleprinter Drive (PWB number PTTA1) connected on the GENIE* Bus. The connection between the printer and the drive controller may be direct or via Modems and phone lines.

Most maintenance information for the Matrix Printer is contained in the vendor manual for the device. (Refer to "4. REFERENCES" of this publication.) Supplementary information is included here to support the vendor manual and to add other troubleshooting information and recommendations relating to the use of the printer with the 4500 computer system.

1.1 Interface

Fig. 1.1 is a block diagram of the Matrix Printer/4500 system interface.

2. PRECAUTIONS

The Matrix Printer has 115 Vac present and should be handled accordingly. Do not pull cords with the power on, and use common sense precautions to avoid an electrical shock. Avoid catching loose clothing or fingers in mechanical parts such as the drive belt or print head.

3. OPTIONS

3.1 Model Numbers

The following are Matrix Printer model numbers:

AMPA21/22 Matrix Printer 300-baud KSR Voltage Interface, 60 Hz/50 Hz

AMPA23/24 Matrix Printer 300-baud KSR Current Interface, 60 Hz/50 Hz

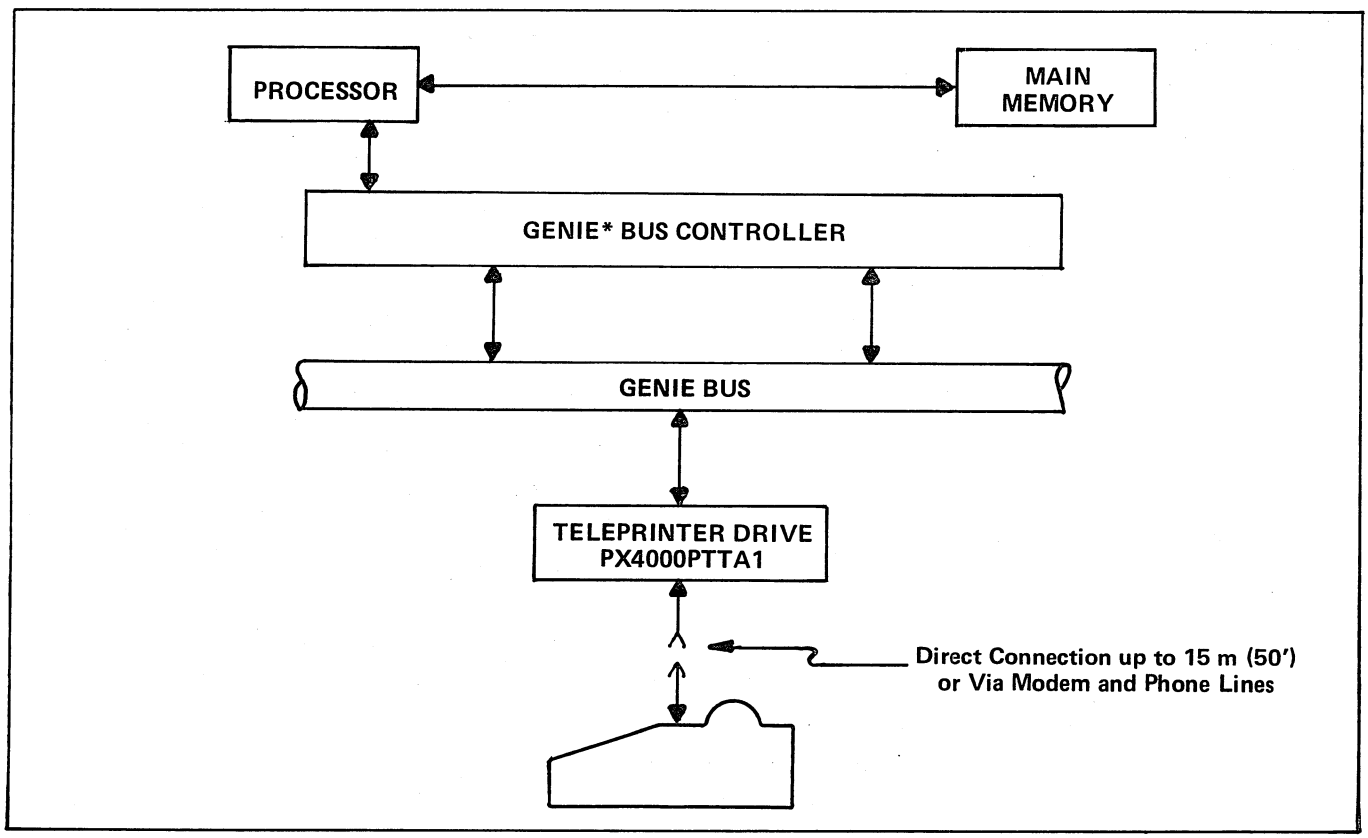

Fig. 1.1 Matrix Printer/4500 System Interface Block Diagram

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AMPA11/12 Matrix Printer 300-baud RO Voltage Interface, 60 Hz/50 Hz

AMPA13/14 Matrix Printer 300-baud RO Current Interface, 60 Hz/50 Hz

AMPB21/22 Matrix Printer 1200-baud KSR Voltage Interface, 60 Hz/50 Hz

AMPB23/24 Matrix Printer 1200-baud KSR Current Interface, 60 Hz/50 Hz

AMPB11/12 Matrix Printer 1200-baud RO Voltage Interface, 60 Hz/50 Hz

3.2 Vertical Tabulation and Form-feed

This option is designed for paper with an 11-inch form length (66 lines per page). The top-of-form position and the vertical tab positions are specified by holes punched in a special tape by the user. Vertical tabulation can also be set from the computer or keyboard. A vertical tab transferred from the computer or generated at the keyboard slews the paper to the top of the next form (page).

3.3 PWA Switch and Jumper Options

There are a number of switch and jumper options in the subsystem. These options are divided into two groups here, with each group defining where (SPI or MPD) the option exists.

3.3.1 SPI Options

Fig. 3.1 shows the jumper and switch settings for the SPI PWA. The pin jumper should be set to either the 300 or 1200 position, as shown. The specific setting should reflect the type of matrix printer. (See heading 3.1.) The device address and switch priority settings can be accomplished using the following guidelines.

Device Address Settings

The SPI device address is selected by nine miniature switches on the controller's PTTA1 board. The switches are labeled AP and A7 through A0, and are set to "0" or "1", as necessary to select a binary number equal to 400g less than the device address, DDD, assigned to the device by the system documentation. Bit AP is set to provide odd parity. For example, if the device address is 401g, the switches are set as follows:

AP	A7	A6	A5	A4	A3	A2	A1	A0	-
0	0	0	0	0	0	0	0	1	-

Switch
Value

Six miniature switches on the PTTA1 board are used to select the relative API priority of the 16 priority levels available on the master or slave bus section the controller is installed on. The switches labeled 0X, 1X, 2X, X0, X1, and X2 are set to one or zero to specify the octal number related to the priority assigned by the system documentation, as follows:

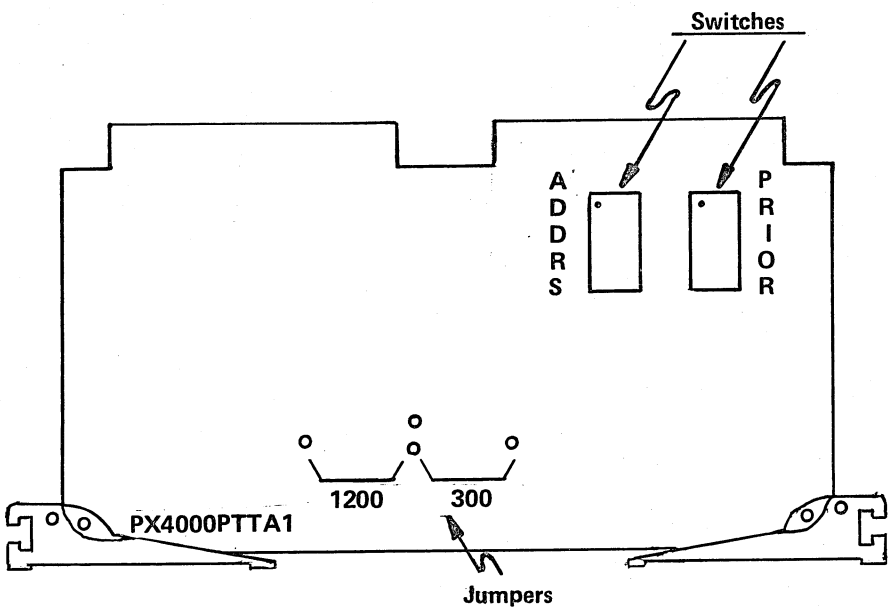

Fig. 3.1 SPI Option Settings

	Priority	Switch Setting
Highest	1	33_8
	2	35_8
	3	36_8
	4	37_8
	5	53_8
	6	55_8
	7	56_8
	8	57_8
	9	63_8
	10	65_8
	11	66_8
	12	67_8
	13	73_8
	14	75_8
	15	76_8
Lowest	16	77_8

3.3.2 MPD Options

There are two PWA's (three, if a current interface) on the MPD that have optional switch settings. These PWA's are the Microprocessor board, the Printer Drive board, and (if current interface) the Current Interface board. Table 3.1 summarizes the switch settings.

4. REFERENCES

The following documents will be of assistance when working on the Matrix Printer subsystem:

- 4500 General Description, PTH-019, Section 8
- Matrix Printer Subsystem Theory, AMPA/B-T
- Test Programs

  4500 System Exerciser, 51191050; Matrix Printer Module Unit Test Program, 51103039

- Matrix Printer Vendor Manual (HIS Italia Manual), 71011433-001

5. COMPONENT LOCATIONS

Locations of operator controls on the Matrix Printer are illustrated in the vendor (HIS Italia) manual.

The Teleprinter Drive board, PX4000PTTA1, is located in a GENIE Bus slot in the CSU or an expansion chassis. The interconnecting cable connects to the "B" field of that card slot and to the rear of the printer.

6. EQUIPMENT AND MATERIALS

Equipment required to maintain the printer is specified in the Maintenance Procedure section of the vendor manual. Metric hand tools are required.

7. PREVENTIVE MAINTENANCE

Preventive maintenance for the printer is specified in the Maintenance Procedures section of the vendor manual. No preventive maintenance is required for the drive board.

8. PERFORMANCE TESTS

At installation, run the Matrix Printer Module with the System Exerciser and other test modules.

For a more comprehensive test, three or more error-free passes through unit T.D. 51103039 are sufficient.

9. ASSEMBLY AND DISASSEMBLY

The vendor manual contains assembly/disassembly instructions for the major components associated with the Matrix Printer.

10. ADJUSTMENTS

The Maintenance Procedures section of the vendor manual contains adjustment instructions for the Matrix Printer.

PRINTER MICROPROCESSOR BOARD SWITCH SETTINGS				
PWA CPU00			DWG. 78119300	
Switch	30 Characters/Second		120 Characters/Second	
S01- 0	OFF-	Don't Care	OFF-	Must
1	OFF-	Var. Baud Select	OFF-	Must
2	OFF-	Must	ON-	Must
3	OFF-	Must	OFF-	Must
4	ON-	Var. Baud Select	OFF-	Must
5		N/A		N/A
6	ON-	Must	ON-	Must
7	OFF-	Must	OFF-	Must
8	OFF-	Not VFU Opt.	OFF-	Not AFF
9	ON-	QWERTY Keys	ON-	On Line @ Pwr. Up
10	OFF-	200 ms Break	ON-	132 Columns
11	ON-	Print Diamond	ON-	Print Diamond
12	ON-	QWERTY Keys	ON-	Keyb'd. Transc.
13	ON-	Must	ON-	Must
14	ON-	VT Enabled	ON-	Not VIP
15	OFF-	Local Print	ON-	Full Duplex
16	ON-	On-Line @ Pwr. up	ON-	Enable V.T.
17	ON-	Upper Case Only	ON-	N/A
18	OFF-	Even Parity	OFF-	Local Print
19	ON-	132 Columns	OFF-	Buffer O.F. Sig.
20	ON-	1 Stop Bit	OFF-	Upper Case Only
21	OFF-	Don't Care	OFF-	Don't Care
22	OFF-	Don't Care	OFF-	Don't Care
23	OFF-	Don't Care	OFF-	Don't Care
24	OFF-	Don't Care	OFF-	Don't Care
25	ON-	No AFF	ON-	No AFF
26	OFF-	Must	OFF-	Must
27	ON-	Must	ON	Must
28	ON-	Must	ON-	Must
29	OFF-	Must	OFF-	Must
30	ON-	Not VIP 7200	ON-	No VFU
31	OFF-	Don't Care	OFF-	Must
32	ON-	Must	ON-	Must

PRINTER UNIT DRIVE BOARD SWITCH SETTINGS (PWA DRIVE 78117135-004)				
S-01	ON-	Must	OFF-	Must
02	ON-	Must	OFF-	Must
03	ON-	Must	ON-	Must
04	ON-	Must	OFF-	Must

PRINTER UNIT CURRENT INTERFACE SWITCH SETTINGS (PWA LOOCU 78118448-001)				
SW01-01	ON-	External Current	ON-	External Current
02	OFF-	External Current	OFF-	External Current
03	OFF-	External Current	OFF-	External Current
04	ON-	External Current	ON-	External Current

Table 3.1 MPD Optional Switch Settings

11. TROUBLESHOOTING

You are likely in this section of the maintenance manual because you have symptoms of a problem relating to the matrix printer. Such symptoms may vary according to the type of control mode (on line, off-line) used. Symptoms in an on-line control mode are a lack of response to operator actions involving the MPD, a system alarm message relating to the MPD, or a lack of action on the part of the MPD when it was expected. Off-line control mode symptoms range from alarm messages (when controlled by an off-line program with alarm message capability) to alarm indicators and inappropriate response following instruction executions at the console. Fig. 11 is a troubleshooting directory that provides a visual guide to use of this section in isolating error sources in any of the three control modes. Subsection 11.1 guides you in interpreting this directory and in locating the corresponding references for further explanations. Subsection 11.2 assists in the interpretation of error and alarm indications.

11.1 Using the Troubleshooting Directory

A check should always be made of the MPD itself when there are error indications relating to the MPD, regardless of the control mode being used. For any type of control response, the MPD must be on line and ready. Refer to 11.2.4 to determine how this can be interpreted.

Subsections 11.1.1 through 11.1.3 contain isolation information for the three types of control modes referenced by Fig. 11. On line is defined as being under RTMOS control. Off line control is defined as being directed by formally issued test programs or by console executed commands. Console executed commands include test loops entered into memory and run in the automatic mode or individual instructions executed in the step mode. Console refers to the Programming and Maintenance Console (P & MC) at the front of the CSU cabinet.

11.1.1 On-Line Isolation

On-line indications of a subsystem failure include system alarm messages or an inappropriate response by the device. There are two basic approaches you can take to these conditions. One is an on-line swap using an acceptable replaceable device, and the other is a gathering of symptoms to be used in making off-line checks.

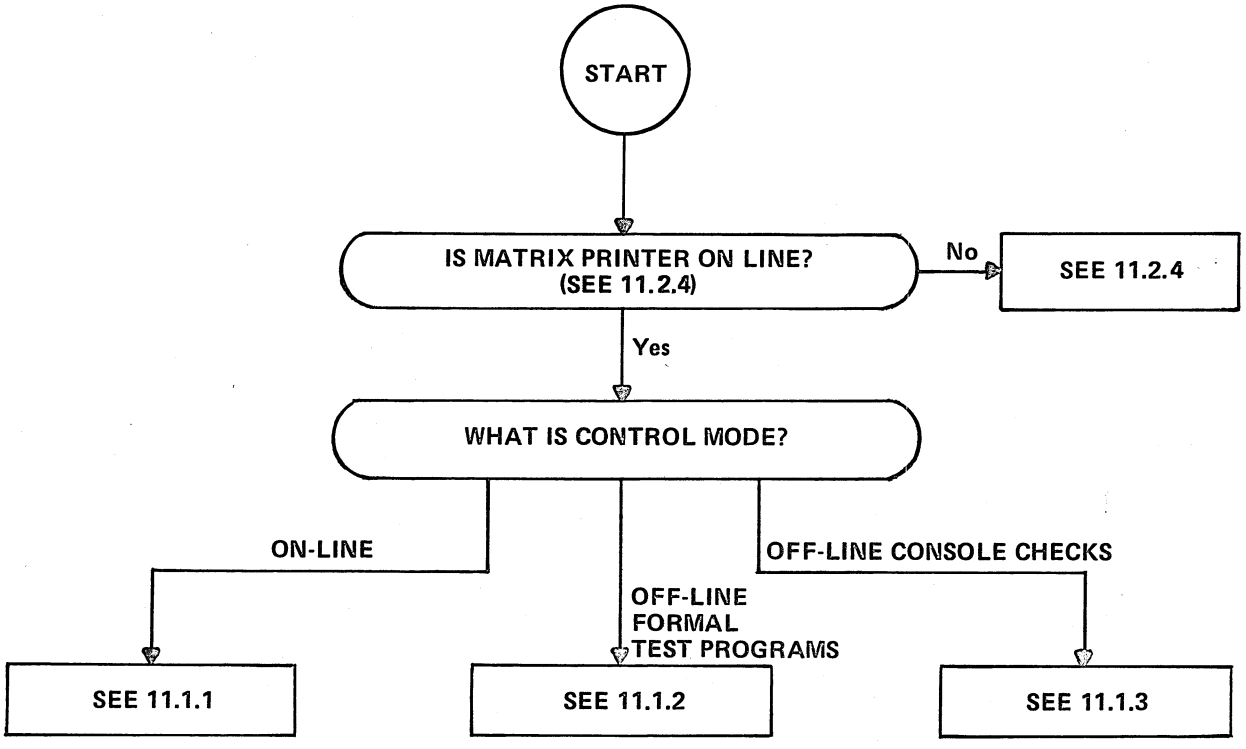

Fig. 11 Trouble Shooting Directory

Swapping MPD's On Line

If you are swapping an MPD on line, be sure that the original device is taken out of service. (See Peripheral In/Out of Service section of the PTS-052 Operator's Manual.) This prevents any inadvertent interrupts from affecting the system. (There is always the possibility of noise spikes being generated on signal lines during disconnection and reconnection of the interface cable, however. Use care not to short any of the interface pins and be prepared for possible interference with system control.)

Matrix Printer devices should not be swapped unless they are replaceable units. Keep in mind the incompatibility of RO (output only) versus KSR (input/output), voltage interface versus current interface, 300 baud versus 1200 baud, and 50 Hz, versus 60 Hz.

Gathering of Symptoms for Off-Line Testing

Make careful notation of whatever indications of malfunction may be available. These symptoms will direct your testing and checking while in the off-line isolation mode. Specifically record or keep a copy of any system alarm messages that occurred while on line, and note what type of system response might have occurred in response to actions at the device.

If the MPD is used as a primary or backup I/O device to call up COS response, note the reaction to pressing the Break button at the keyboard. Should a disc be used as the bulk device, a bulk transfer (likely causing disc head movement) occurs to transfer COS to memory. Such a response indicates program recognition of an interrupt from the subsystem.

If you are familiar with the RTMOS* control tables and flags pertaining to the device, and how to have the information dumped, gather that information or try to have a system programmer obtain it for you. (This information should be gathered as soon as possible after the failure indication.) If necessary, attempt to recreate the failure condition and get the information. Refer to 11.2.1 for interpretations of on-line alarm messages.

After symptoms of the on-line malfunctions have been gathered, proceed to off-line testing by formal test programs or by console checks. Off-line testing by the test programs requires an additional I/O device in addition to the one being tested. The additional device is required for interactive selection and alarming. Should there not be an additional device available, it may be necessary to perform console checks.

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11.1.2 Off-Line Formal Test Program Isolation

Off-line formal test programs are the T&D Program (51103039) and the System Exerciser Program (51191050). Either of these require an I/O device in addition to the one being tested. Should there not be an additional one available, it will be necessary to resort to hand-loaded test loops or console-executed checks of the device.

Assistance in operating and interpreting the T&D and System Exerciser programs is provided by publications ATPG-I and SEX-I, respectively. Alarm messages should be examined to determine the type of operation taking place and the error test indications given. This information should be correlated with that given under 11.2.3.

Running the T&D Program

Set the printer to "ON LINE" and "DATA SET READY" by pushing the ON LINE button twice. Both the ON LINE and DATA SET READY mode lights should be ON before continuing.

NOTE

A second printing device must be used as a logging printer, otherwise the T&D Program will not run all the applicable tests.

Load the T&D Program 51103039 into the test computer and verify the proper hand loaded parameters as follows:

Location	Value	Remarks
1201	0000 4101	Logging Device Adr.
1202	0000 4101	
1203	0000 4102	Matrix Printer Input Adr.
1204	0000 0224	TIM API
1205	0000 0225	Echo
1206	0000 4103	Printer Output Adr.
1207	0000 0226	TOM API
1210	0000 0227	Echo
1213	0000 000-	Options to be tested
		Bit 0 - Current Drive
		Bit 1 - Must be set
		Bit 2 - Must be set
1215	0000 0003	Halt at end of pass 3.

Initial Printer Tests:

Start the T&D Program and select the following console switch options:

Console Switch Image - 1320 **00 octal

CS21	Halt after error
CS19	Manual Intervention Tests
CS18	Pause at end of pass
CS16	Inhibit repeating test after failure
*CS09	Device is KSR
*CS08	1200 Baud Rate Device

Enable Interrupts and run one pass of the following tests.

	KSR 1200		KSR 300		RO 1200		RO 300	
	Voltage	Current	Voltage	Current	Voltage	Current	Voltage	Current
Tests	0	0	0	0	0	0	0	0
	1	1	1	1	1	1	1	1
	2	2	2	2	2	2	2	2
	4	4	3	3	4	4	3	3
	5	5	5	5	5	5	5	5
	7	7	6	6	7	7	6	6
	9	9	9	9	9	9	9	9
	10	10	10	10	11	12	11	12
	11	12	11	12	15	15	15	15
	14	14	14	14	16	16	16	16
	15	15	15	15	17	17	17	17
	16	16	16	16				
	17	17	17	17				

Visually check the printed data for errors, and proper print characters.

Manual Tests:

A. Keyboard Test (KSR Models):

Run the program in the single test mode for keyboard inputs (Test 14). Console switch image 12041*16 octal. (*) = set switch 8 if device is 1200 baud.

When logging printer requests a character string, input all printable keys in upper case (do not use shift key), followed by a line feed (LF) and carriage return (RETURN). The program should print out a line of the same characters.

Repeat the above step, but use the shift key and input all lower case characters. (Letters will be in capitals only).

B. Print Position Indicator (KSR Models):

Using Test 14 as above, input a character string of 10 characters, checking the print position indicator after each one. Input a string of ten more characters and check the indicator every ten characters up to 132.

C. Audible Alarm (Bell):

The audible alarm is a high-pitched "beep" of ½ second duration.

KSR devices: The bell can be activated through the keyboard as in Step "A" above.

RO devices: The bell can be activated from the CPU console by executing the following program instructions:

D = Device Output Address

Location	Instruction	CMD	Remarks
100	4000 0035	LDK	Enable Code
101	2502 4103	OPR	
102	4000 0007	LDK	Load Bell Code
103	2504 4103	OUT	Activate Bell
104	1407 7777	BRU	Loop

Step through the program loop. The bell should sound each time through.

Extended Run:

Restart the T&D Program and select the following console switch options:

Console Switch Image = 1000 **00 octal

CS10	Inhibit Tests 16 & 17
*CS09	KSR Printer
*CS08	1200 Baud Rate Device

Enable interrupts and run 3 passes of the following tests (Test 0 on the first pass):

1200 Baud		300 Baud	
Voltage	Current	Voltage	Current
Tests 1	1	1	1
2	2	1	2
4	4	3	3
7	7	6	6
9	9	9	9

Visually check the printed data for errors per the program write-up and Fig. 11.

11.1.3 Off-Line Console Checks

Off-line console checks refers to execution of test loops or step-sequenced instructions loaded and executed from the Programming and Maintenance Console (P&MC). Although such checks cannot duplicate on-line conditions and interactions, they can provide a well-controlled check of the basic operational abilities of the subsystem. The following information assists you in performing checks of this type. The discussion is divided into categories of input, output, and interrupts.

11.1.3.1 Output Operational Checks

The defined sequence of command executions required to perform a check of an output operation involving this subsystem are as follows:

- Clear channel to remove any residual errors or operational hangups
- Set Channel Busy
- Transfer Data
- Clear Channel Busy

There is quite a bit of flexibility possible in creating a test loop to check output operations. The bulleted items above listed the required sequence of control, but you may wish to write a hand loop that includes jump tests at various places to look for specific responses. The following checks indicate what the normal response of jump tests should be when executing the defined control sequence.

Lock out interrupts at the P&MC prior to starting. Follow the checks in the sequence listed. Select jump tests as desired.

Clear Channel

This can be accomplished by several methods, as defined under 11.2.5. An abort of the specific channel is recommended to localize the clearing effect. Following the clear operation, the following jump checks should yield the indicated results:

JCB: Not Busy (P+1) JDR: Ready (P+2)

JNE S'=0: No Error (P+2) JNE S'=2: No Error (P+2)

JNE S'=6: No Error (P+2)

> **NOTE**
>
> Clearing the channel or the entire system will not remove an alarm condition from the MPD itself. If there is an alarm from the MPD, it will still be indicated by the JNE S'=0 check. It will not be indicated by the JNE S'=2 check until the channel busy is set.

Set Channel Busy

Execute an OPR command, addressed to the Output channel, with a 177_8 (DEL) code in the A-register. This should cause the channel busy to set. Jump tests should yield the following results:

JCB: Busy (P+2) JDR: Ready (P+2)

JNE S'=0: No Error (P+2) JNE S'=2: No Error (P+2)

JNE S'=6: No Error (P+2)

> **NOTE**
>
> MPD alarm can now be detected by either JNE S'=2 (since channel now busy) or JNE S'=0.

Transfer Data

Place a printable character code in the least significant byte of the A-register and execute an OUT command addressed to the Output channel. There should be a character printout at the MPD. The Ready line will pulse not ready during the transfer and then return to ready. Jump tests should yield the following results:

JCB: Busy (P+2) JDR: Ready (P+2)

JNE S'=0: No Error (P+2) JNE S'=2: No Error (P+2)

JNE S'=6: No Error (P+2)

NOTE

JNE S'=2 error indicates an MPD alarm. JNE S'=6 error indicates a Data Error. JNE S'=0 indicates either. See 11.2.3 for interpretation.

Clear Channel Busy

Place 024_8 (DC4 code) in the least significant byte of the A-register and execute an OUT command addressed to the Output channel. Jump tests should yield the following results:

JCB: Not Busy (P+1) JDR: Ready (P+2)

JNE S'=0: No Error (P+2) JNE S'=2: No Error (P+2)

JNE S'=6: No Error (P+2)

NOTE

JNE S'=0 error indicates MPD alarm. JNE S'=2 and S'=6 should not permit error indication since channel busy is no longer set. See 11.2.3 for error/alarm interpretations.

11.1.3.2 Input Operational Checks

The defined sequence of command executions required to perform an input operation is as follows:

- Break - Required to trigger initial interrupt for program response; not required for programs not using interrupts.
- Set Channel Busy
- Input Data - This will follow actual keying of data at the MPD.
- Clear Channel Busy - Done by carriage return at the MPD, triggering an end-of-record interrupt.

Like the output operational checks, there are many possibilities of programming test loops. The following is a description of the required control actions and the normal results if jump commands were to be executed following them. Lock out API's during the sequence and follow in the order listed. Select jump tests as desired.

Break

See subsequent interrupt description.

Clear Channel

This can be accomplished by several methods, as defined under 11.2.5. An abort of the specific channel is recommended to localize the clearing effect. Following the clear operation, the following jump tests should yield the indicated results:

JCB: Not Busy (P+1) JDR: Ready (P+2)

JNE S'=0: No Error (P+2) JNE S'=2: No Error (P+2)

JNE S'=6: No Error (P+2)

NOTE

Clearing the channel or the entire system will not remove an alarm condition from the MPD itself. If there is an alarm from the MPD, it will still be indicated by the JNE S'=0 check. It will not be indicated by the JNE S'=2 check until the channel busy is set.

Set Channel Busy

Place 002_8 (Start of Text) code in the least significant byte position of the A-register. Execute an OPR command addressed to the Input channel. Jump tests should yield the following results.

JCB: Busy (P+2) JDR: Ready (P+2)

JNE S'=0: No Error (P+2) JNE S'=2: No Error (P+2)

JNE S'=6: No Error (P+2)

NOTE

MPD alarm can now be detected by either JNE S'=2 (since channel busy set) or JNE S'=0. See 11.2.3 for error/alarm interpretation.

Transfer Data

Type an alphameric character at the MPD. Execute an IN command addressed to the input channel. The code representing the character should appear in the least significant byte of the A-register. Jump tests should yield the following results after depressing the key and then after doing the IN command execution.

JCB: Busy (P+2) for both

JNE S'=0: No Error (P+2)

JDR: Ready (P+2) after pressing key. Not ready (P+1) after IN.

JNE S'=2: No Error (P+2)

JNE S'=6: No Error (P+2)

NOTE

See 11.2.3 for error/alarm interpretation. A printout at the device of character keyed means that data is being successfully echoplexed. Echoplexing is the deserializing (receipt and hold) of data at the SPI and then returning (serialized transmit) it to the device.

Clear Channel

Press the Carriage Return key at the MPD. This should clear the channel busy at the input channel. Jump tests of the Input channel should yield the following results:

JCB: Not Busy (P+1)

JDR: Ready (P+2)

JNE S'=0: No Error (P+2)

JNE S'=2 No Error (P+2)

JNE S'=6: No Error (P+2)

NOTE

JNE S'=0 error indicates MPD alarm. JNE S'=2 and S'=6 should now be ineffective (no error report) since the channel is not busy. See 11.2.3.

11.1.3.3 Interrupt Checks

It is possible to execute instructions in a step mode at the Programming and Maintenance Console that would trigger interrupts from the SPI. They would never be serviced in the step mode, however, since the clock interrupt would always be pending and take priority for service.

A full response check requires a test program running in the automatic mode, with appropriate interrupt control and vector response included. (Example: TIM/TOM test loops using a device emulator are included in the ACPUGBC-M maintenance publication for the GENIE Bus Controller. Device addresses corresponding to the SPI input and output channels would have to be used and corresponding interrupt vectors would have to be set up.)

You can check actual triggering of interrupts at the SPI in the step mode so that an oscilloscope or meter could be used to monitor the actual circuits to determine if they generate interrupts under the proper conditions. The following information assists in such checks.

Subsystem Interrupts and Conditions Generating Them

There are two basic interrupt types for each (input and output) channel at the SPI Data Exchange (DEI) and End-of-record (EOR). DEI interrupts basically indicate when data can be transferred and result in a TOM (for output) or TIM (for input) control response from the corresponding interrupt vector for the channel. DEI's are non-inhibitable interrupts for the SPI, while EOR's are inhibitable interrupts.

EOR interrupts are basically used to solicit control response from the program. They are used, for example, to trigger input sequences or to terminate both input and output sequences. The following text defines conditions required to trigger the DEI and EOR interrupts for input and output channels.

Input:

Select API lockout at the P&MC. Ensure MPD is on line and available. Clear the input channel prior to starting the sequence. After clearing the channel, check B65 high for DEI and B12 high for EOR, to ensure there are no residual interrupts. If there are, either the clear is not working or there is a problem with the SPI.

1. Press the Break button at the MPD.

   Should generate EOR. Pin B12 at backpanel of SPI board slot should go low.

2. Execute OPR with 177_8 code in A-register.

   Channel Busy should set. Pin B66 will go high.

3. Type a character at the MPD.

   Results in a DEL. Pin B65 should go low.

Ordinarily, the EOR and DEI interrupts generated by steps 1 and 3 would be serviced, but will not be generated since interrupts are locked out. It is now necessary to clear the existing EOR interrupt to check for the final EOR. This can be done by again clearing the input channel and then repeating step 2. Proceed to the next step.

4. Hit the carriage return at the MPD keyboard.

   Results in an EOR. Pin B12 should go low.

Output:

Select API lockout at the P&MC. Ensure MPD is on line and available. Clear the output channel prior to starting the sequence. After clearing the channel, check B08 high for DEI and B61 high for EOR to ensure there are no residual interrupts. If there are, either the clear is not working, or there is a problem with the SPI.

1. Execute OPR with 177_8 code in A-register.

   Sets channel busy (pin B23 high) and generates DEI (pin B08 low).

In normal operation, the DEI generated by step 1 would be serviced. It will not be serviced in this situation because we have interrupts locked out. We can check the DEI interrupt for a character output by clearing the channel and performing the following step.

2. Place a printable character in the least significant byte of the A-register. Execute an OPR to the Output channel. The character should print at the MPD and a DEI should be triggered. Check pin B08 for a low level.

3. Execute an OUT command (addressed to the Output channel) with an 024_8 (DC4) code in the A-register. Check pin B61 for a low level (EOR).

11.2 Error/Alarm Interpretations

Several program-testable error lines and a device alarm line are used in communicating error detections to the program control and to the user. The device alarm line connects to the Alarm line at the Programming and Maintenance Console and may not be visible in the on-line mode or during some off-line test program sequences since it can be cleared by some program control actions. The error line testing is also not directly visible to the user, but results of such tests usually result in system alarm messages. The following descriptions under the 11.2 heading will assist you in interpreting which types of error or alarm indications you should expect in the different control modes.

11.2.1 On-Line System Alarms

On-line detection of errors and alarms are reported as system alarm messages or as flags to requesting programs. System alarm messages include Corrective Action Program messages and Trap Handler Messages. Request programs, which communicate with RTMOS drivers to request input/output control sequences may provide the user with alarm messages based upon flags sent to them after servicing of the request. Since each program handles such error messages in their own manner, they are not discussed here. You may wish to refer to Section 3 of the RTMOS Application Manual (PTS-051) to determine the flag reporting sequence. CAP and Trap Handler messages are standardized and are described in Special Discussion 13 of the RTMOS Application manual.

CAP is called into service if the input or output driver for this subsystem runs into difficulty while trying to service a user request. Generally speaking, the driver makes checks before, during, and after the actual transfer operations involving the device. Any detected error indication causes CAP response. CAP then checks for specific error line conditions and reports the results, either as a system alarm message or as a flag error to the request program.

CAP alarm messages for this subsystem include:

- Data Error - Detected by a JNE S'=6 check of the involved channel (See 11.2.3.)

- Device Failure - Detected by a JNE S'=2 check of the involved channel. (See 11.2.3.)

- Device Out-Of-Service - Detected by a JNE S'=0 check. (See 11.2.3.) This message typically is indicated if neither the JNE S'=6 or S'=2 error line was true during CAP checking. This could occur if there was a residual failure at the SPI when the driver was entered or if a diagnostic countdown occurred during an output operation.

11.2.2 Off-Line Test Program Messages

Alarms and error messages during the execution of formal test programs are described by publication ATPG-I (for the 51103039 Matrix Printer Test Program) and by publication SEX-I (for the System Exerciser, 51191050). Interpretations of these messages can be correlated with the specific error tests and alarm line checking described under 11.2.3 of this publication.

11.2.3 Error Tests (JNE) and Alarm Line

Error detections occur at all levels of the subsystem and even at the CPU, but error information pertaining to this subsystem is consolidated at the SPI. The reporting of the results of these checks is accomplished by JNE tests and by a device alarm line. The JNE tests, which sample the status of error lines at the SPI, indicate status in the form of a branch result to the JNE execution. Error status is indicated if the Program Counter (P) is incremented by plus 1 (error) or plus 2 (no error). The alarm line, however, is connected to a visible indicator at the Programming and Maintenance Console. An alarm is clearly visible while executing step checks, but may be extinguished before being seen while in the on-line control mode. Aside from observable device malfunctions or by indications provided by signal tracing, the jump tests and alarm line are the only indications of the subsystem operation.

Fig. 11.1 shows the consolidation of the status and alarm checks at the SPI. The table at the bottom of the figure is a breakdown of conditions that cause or clear each of the possible JNE tests that can be addressed to the input and output channels of this subsystem. The table also lists conditions for enabling and clearing the device alarm line that is connected to the P&MC indicator. The other portion of the figure is a block diagram of the subsystem, showing the interface signals involved in the formulations, as well as the status information and alarm line being reported via the GENIE Bus. The information contained in that diagram is discussed by the following text in three segments that deal with the MPD, the SPI, and the GBC, each of which are originators of fault indications that are consolidated at the SPI.

Error Conditions Reported by the MPD to the SPI

The MPD performs some checking of its internal condition and of its operation. Basically, these checks are of the paper supply, the carriage motion, and the print head. (Refer to the vendor manual for the device for specific information on the checks made.) Any of these conditions will render the MPD unavailable for operation and will be reported for program testing via the JNE commands. Generally speaking, the MPD is indicated unavailable by the JNE S'=2 line. It is also indicated unavailable by the JNE S'=0 line, since that line includes errors from S'=2 or S'=6.

Both interface options (voltage and current) supply device status from the MPD to the SPI via the receive lines. In addition, the voltage interface connects device status signals to the SPI. Even though the current interface does not include the device status signals for SPI monitoring, the resultant status information from either interface remains virtually the same. This occurs since any MPD condition causing an indication via the device status lines is also reported by a break via the receive lines.

The receive lines communicate status (in addition to data) to the SPI and are connected between the MPD and SPI regardless of the type of interface connnection. The device status lines are used only for the voltage interface connection. There are actually two device status signals, DTR and RTS, which are labeled DSR and CON at their connection to the SPI, as shown on Fig. 11.1.

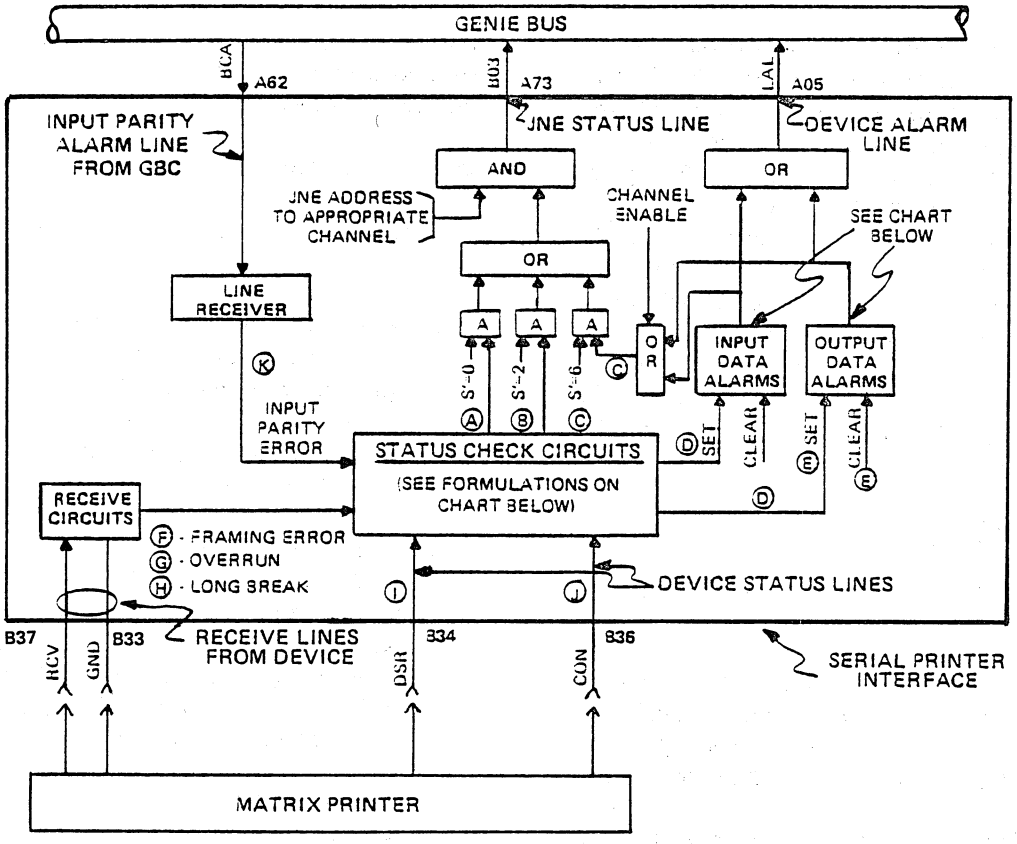
Fig. 11.1 combines a formulation table, which indicates the conditions that cause or clear jump-testable status lines or alarm lines at the SPI, with a block diagram showing the interface signals from which the formulations are derived. The signals from the MPD that affect the formulations are the DSR and CON signals just mentioned, and break signals communicated via the receive lines. The significance of the break signals is a function of the length of the break.

Break is the absence of a mark signal on the data receive lines. A break of up to one character length is accepted as data (i.e., all zeros). A short break, caused by pressing the MPD Break button, triggers an input interrupt when the input channel is busy. Any break beyond 260 ms is recognized as a long break. A long break indicates the device is unavailable (i.e., not on line and ready) or a disconnected interface cable.

Error Checks by GBC Reported to SPI

The GBC checks parity on information transferred to it from the SPI. This occurs under the following conditions:

- Input data transfers - the GBC checks for odd parity on the data transferred from the SPI to the GBC during IN instruction or TIM control word executions. Since the SPI assigns parity to the data received from the device, either the SPI or the GBC is at fault when an error of this type is detected. The error is reported by asserting a low level on the BCA line (see Fig. 11.1) at completion of the transfer.



STATUS CHECK FORMULATIONS
(SEE STATUS CHECK CIRCUITS AND DATA ALARM CIRCUITS ON ABOVE ILLUSTRATION)

	CORRESPONDING CIRCUIT FROM ABOVE	JNE SUB-CODE REQUIRED	CONDITIONS ENABLING ERROR STATUS FOR CIRCUITS	CONDITIONS TO CLEAR ERROR STATUS
If Input Channel Addressed	Ⓐ (Test Line 0)	Input Channel S' = 0	Ⓐ = Long Break Ⓗ + CON Ⓙ + B + C	Removal of Alarm Condition
	Ⓑ (Test Line 2)	S' = 2	Ⓑ = Input Channel Busy · (Long Break Ⓗ + DSR Ⓘ + CON Ⓙ	Operate to Input Channel + SCLR + GCLR + Abort to Input Channel
	Ⓒ (Test Line 6)	S' = 6	Ⓒ = Input Channel Busy · (FRE Ⓕ + Overrun Ⓖ + IN PE Ⓚ)	Operate to Input Channel + SCLR + GCLR + Abort to Input Channel + Reset Alarm + Long Break
	Ⓓ (Input Data Alarm)	Not JNE Testable	Same as for Input Test Line 6 Above	Same as for Input Test Line 6 Above
If Output Channel Addressed	Ⓐ (Test Line 0)	S' = 0	Ⓐ = Long Break Ⓗ + DSR Ⓘ + CON Ⓙ + B + C	Removal of Alarm Condition
	Ⓑ (Test Line 2)	S' = 2	Ⓑ = Output Channel Busy · (Long Break Ⓗ + DSR Ⓘ + CON Ⓙ)	Operate to Output Channel + SCLR + GCLR + Abort to Output Channel
	Ⓒ (Test Line 6)	S' = 6	Ⓒ = Output Channel Busy · (FRE Ⓕ + Overrun Ⓖ + IN PE Ⓚ)	Operate to Output Channel + SCLR + GCLR + Abort to Output Channel + Reset Alarm + Long Break
	Ⓔ (Output Data Alarm)	Not JNE Testable	Same as for Output Test Line 6 Above	Same as for Output Test Line 6 Above

Fig. 11.1 Error/Alarm Checking

- Interrupt Acknowledge - the GBC checks for odd parity on data transferred from the SPI to the GBC during acknowledgement of interrupt requests from the SPI. (See prior discussion of interrupt checks to determine when interrupts occur.) The parity assigned is a function of the device address and device address parity switches selected at the SPI. Check that these switches are set for odd parity. Note whether the switches are installed with correct polarity of the reference dots on the switches and board. This alarm is also reported by the BCA line mentioned above. This error could occur anytime there is an interrupt acknowledgement, for either input or output channel.

Error Checks Internal to SPI

The SPI makes the following checks of data during input operations:

- Framing error - occurs if a break signal occurred on the receive line for a time period exceeding the length of a character transmission from the MPD. Should the break continue to the duration of a long break (approximately 260 ms.), the alarm would be cleared. This alarm occurs if a short break (break button pressed) occurs while the channel is busy.

- Overrun - occurs if a new character is transmitted to the SPI (by a key selection at the MPD) before the previous one was input to the CPU via an IN instruction or TIM control word execution.

11.2.4 Device Ready

The device must be in an on-line condition (i.e., power on, but not in local or standby mode). For RO versions, there will be two lights lit: on-line and Data Set Ready; for KSR versions only the on-line light is lit. Internal checks by the MPD, as mentioned under 11.2.3, can cause the MPD to go to a standby or power off mode. Normal conditions that cause device not ready are a disconnected power cord, a paper low condition, or the MPD not switched to the on-line mode.

11.2.5 Clear Signals

The following are clear methods available that affect the SPI:

- Alarm Clear - clears all alarm conditions (except internal GBC check alarms) reporting to the Alarm light, including the Date Error alarms detected by a JNE S'=6 to the input and output channels. It does not clear a device alarm; the conditions causing a device alarm must be removed.

- Device Clear - generated as a result of an Abort command addressed to the SPI address. Abort to the Input channel clears that channel, including Channel Busy, Data Not Ready, and the Data Error. Abort to the Output channel clears corresponding conditions for that channel. This signal is also asserted when either of the following two clears are generated.

- GCLR - GENIE Bus Clear is generated when an Abort 4070 is executed. It clears the GBC and all device controllers on the Bus. Device controllers on the bus are cleared in the manner described by Device Clear. This signal is also generated by the following SCLR condition.

- SCLR - System Clear is generated whenever the system powers up or whenever a Reset/# is pressed at the P&MC. It clears all system control, including those mentioned by the above clear signals.

12. PARTS

Refer to the Illustrated Parts Catalog section of the vendor manual for Matrix Printer parts information.

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